What is claimed is:

1. An overlapping command committing method of dynamic cycle pipeline, for a chip having pipeline structure, comprising the following steps:

(a) reading the command from a command buffer and storing it in a command register;

(b) decoding the command;

(c) preprocessing operators of the command, preparing initial operators of each stage of the pipeline, and storing them into a initialization register;

(d) judging whether the pipeline is not full, if it is not full, directly inserting a new command and then ending; otherwise, waiting for an exiting signal from the command in the pipeline in the last pipeline period before exiting;

(e) after receiving the exiting signal, judging whether there is command relevance between the new command to be inserted and the old command to exit, if yes, then inserting the new command after the old command exit, and then ending; otherwise, performing the next step;

(f) when the old command is in the last cycle of the pipeline, committing the new command to the pipeline.

2. The command committing method of Claim 1, characterized in that the Step (b) also includes a step of judging whether there is illegal command, if there is, then deleting the illegal command and returning to Step (a); otherwise, conducting the next step.

3. The command committing method of Claim 2, characterized in that said illegal command includes: the instructions with incorrect command code and/or carrying unreasonable command parameters.

4. The command committing method of Claim 1 or 2, characterized in that the exiting signal is released before two stages when the new command enters the pipeline stage.

5. The command committing method of Claim 1 or 2, characterized in that the command relevance means that the new command and the old command cannot share the hardware processing module in the same one pipeline stage.

6. The command committing method of Claim 1, characterized in that in the Step (e), it is also judged in which stage of the pipeline stage switch shall be conducted for the new and old commands, and the field switch is completed in the corresponding pipeline stage where the new and old commands overlaps.

7. The command committing method of Claim 1, characterized in that in the Step (e), it is also judged whether there is any field conflict between the new command and the old command, if there is, then the field of the new command is added into the pipeline when committing, while the field of the old command enters into the field branch and maintains until the last time that the old command uses this field; in case there is no field conflict, the field switch is conducted in the corresponding pipeline stage after committing.

8. The command committing method of Claim 1, characterized in that in the Step (c), it is required to provide the initial status of all kinds of commands at the entry to the pipeline.

9. The command committing method of Claim 1, characterized in that the said commands include reading/writing memory commands, reading/writing control register commands and various searching commands.

10. A chip on which the method according to Claim 1, 2, 3, 6, 7, 8 or 9 is carried out having the cycle pipeline structure, comprising: interface of host computer, input buffer, command processing unit, and result unit; the command processing unit comprises: command interpreter and pipeline performing unit; characterized in that the command interpreter further comprises: command buffer controllers, command register, processing unit of operator, pipeline initialization register and control automaton, which are connected in order; the control automaton controls the command buffer controller to read a command from the command buffer, and stores the command into the command register; the control automaton decodes the command, and controls the processing unit of operator to prepare initial operators of each pipeline stage according to the type of the command, and stores them into the pipeline initialization register.